**In the Claims**:

**Claim 1 (previously presented):** An imager cell comprising:

a photoreceptor;

a sense node; and

a pinned transfer gate formed by an implanted P type region within an implanted N type transfer region, the implanted P type region being pinned to a potential of a P type substrate, wherein the P type substrate surrounds the N type transfer region, and wherein the transfer gate is disposed to transfer charge between the photoreceptor and the sense node.

**Claim 2 (canceled).**

**Claim 3 (original):** An imager cell as defined in claim 1, further comprising a photoreceptor readout gate disposed above the photoreceptor.

**Claim 4 (original):** An imager cell as defined in claim 1, wherein the photoreceptor comprises a photogate.

**Claim 5 (original):** An imager cell as defined in claim 1, wherein the photoreceptor comprises a photodiode.

**Claim 6 (original):** An imager cell as defined in claim 1, further comprising a reset transistor disposed to reset the sense node.

**Claim 7 (original):** An imager cell as defined in claim 1, further comprising an output amplifier coupled to the sense node.

**Claim 8 (original):** An imager cell as defined in claim 7, wherein the output amplifier is a source follower amplifier.

**Claim 9 (original):** An imager cell as defined in claim 3, further comprising a readout clock connection coupled to the photoreceptor readout gate.

**Claim 10 (original):** An imager cell as defined in claim 9, further comprising control circuitry coupled to the readout clock connection, the control circuitry supplying a photoreceptor readout clock.

**Claim 11 (original):** An imager cell as defined in claim 10, wherein the photoreceptor readout clock is characterized by a V+ level applied during an integration period, and a V- level applied during a transfer period.

**Claims 12-71 (canceled).**

**Claim 72 (new):** An imager cell comprising:

a photoreceptor, wherein the photoreceptor comprises a photogate;

a sense node; and

a pinned transfer gate formed by an implanted P type region within an implanted N type transfer region, the implanted P type region being pinned to a potential of a P type substrate, wherein the P type substrate surrounds the N type transfer region, and wherein the transfer gate is disposed to transfer charge between the photoreceptor and the sense node.

**Claim 73 (new):** An imager cell comprising:

a photoreceptor, wherein the photoreceptor comprises a photodiode;

a sense node; and

a pinned transfer gate formed by an implanted P type region within an implanted N type transfer region, the implanted P type region being pinned to a potential of a P type substrate, wherein the P type substrate surrounds the N type transfer region, and wherein the transfer gate is disposed to transfer charge between the photoreceptor and the sense node.

**Claim 74 (new):** An imager cell comprising:

a photoreceptor;

a sense node;

a reset transistor disposed to reset the sense node; and

a pinned transfer gate formed by an implanted P type region within an implanted N type transfer region, the implanted P type region being pinned to a potential of a P type substrate, wherein the P type substrate surrounds the N type transfer region, and wherein the transfer gate is disposed to transfer charge between the photoreceptor and the sense node.

**Claim 75 (new):** An imager cell comprising:

a photoreceptor;

a sense node;

an output amplifier coupled to the sense node; and

a pinned transfer gate formed by an implanted P type region within an implanted N type transfer region, the implanted P type region being pinned to a potential of a P type substrate, wherein the P type substrate surrounds the N type transfer region, and wherein the transfer gate is disposed to transfer charge between the photoreceptor and the sense node.

**Claim 76 (new):** An imager cell as defined in claim 75, wherein the output amplifier is a source follower amplifier.